REMARKS

Claims 1 and 11 have been amended to call for providing a register with a different indicator assigned to each of a plurality of central processing units. In other words, each central processor unit has its own indicator. No such system is described in the cited reference. The system may, for example, facilitate access to a common resource wherein the availability of the resource to any given processor may be indicated by the indicator.

The material in the Abstract, column 2, lines 3-32, Figures 1-13, and column 14, lines 18-25, has no such dedicated indicator and, therefore, cannot meet the claim limitations. For example, the material at column 4 indicates that the priority scoreboard issues an available signal according to priority processing. The priority scoreboard checks a scoreboard bit of the requested register. But this clearly refers to a scoreboard bit for a register, not a different scoreboard bit dedicated for each of a plurality of processors.

Claim 18 calls for a first register including general purpose second registers accessible by a plurality of processing units. One said second register indicating whether data in said first register is available for a given one of the plurality of central processing units. As discussed above, the cited art does not include a second register to indicate when the first register can be accessed by a given processing unit.

Therefore, reconsideration of the rejection is respectfully requested.

Respectfully submitted,

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Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Ste. 100
Houston, TX 77024
713/468-8880 [Phone]
713/468-8883 [Fax]

Attorneys for Intel Corporation